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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,813	11/29/2001	James W. Allen	AUS920010911US1	5267

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Gregory W. Carr
Carr & Storm, L.L.P.
670 Founders Square
900 Jackson Street
Dallas, TX 75202

EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,813	ALLEN, ET AL.	
	Examiner	Art Unit	
	Clifford H Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 7/19/2004. Currently claims 1-14 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-4, 7, 9-10, and 13-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The recitation of a "selected processor" is unclear because the implication of a selection is not positively recited.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Munguia (US 6081859) in view of Keller (US 2004/0024945).

Regarding claims 1 and 7, Munguia discloses an arbiter that varies a time between a request for the switched system resources as a function of a number of requests the system indicates to be retried (e.g., col. 7, lines 18-25). Munguia discloses keeping track of latency times of selected processors, but does expressly consider the option of not tracking individual latency times; however this feature is disclosed by Keller. Keller discloses a function of a plurality of requests, without keeping track of latency times of any selected processor (e.g., para. 43).

It would have been obvious to combine Keller with Munguia because Keller teaches simpler implementations of determining when to decrease latencies using a statistic of previous latency data, which statistic was disclosed by Munguia but with the additional feature of tracking individual latency times. Therefore it would have been obvious to one of ordinary skill in the art to combine Keller with Munguia to obtain the claimed invention.

Regarding claims 2 and 8, Munguia also discloses first increasing the time between requests until the system no longer indicates to retry the request and the bus arbiter (e.g., compare Figures 3A and 3B), then decreasing the time between requests after a number of requests processed without the system indicating to retry any requests (e.g., col. 9, lines 28-31).

Regarding claims 3, 9, and 13, Munguia discloses increasing a time between a request from a microprocessor connected to the switched system to use resources of a switch until the switch can process the request (e.g., Figure 3); and decreasing the time between the requests from the microprocessors connected to the switched system to use resources of the switch as a function of some number of requests processed without the bus arbiter having to increase the time between requests from the microprocessors connected to the switched system (e.g., col. 9, lines 28-31).

Munguia discloses keeping track of latency times of selected processors, but does expressly consider the option of not tracking individual latency times; however this feature is disclosed by Keller. Keller discloses a function of a plurality of requests, without keeping track of latency times of any selected processor (e.g., para. 43).

It would have been obvious to combine Keller with Munguia because Keller teaches simpler implementations of determining when to decrease latencies using a statistic of previous latency data, which statistic was disclosed by Munguia but with the additional feature of tracking individual latency times. Therefore it would have been obvious to one of ordinary skill in the art to combine Keller with Munguia to obtain the claimed invention.

Regarding claims 4 and 10, Munguia discloses issuing at least one request from the microprocessor to the system switch (e.g., col. 7, lines 63-64); responsive to a signal from the system switch indicating it lacks resources to process a command, increasing the number of bus clocks to wait between issuance of requests from microprocessors by the number of bus clocks defined as the first parameter; waiting the

increased number of bus clocks between issuance of requests to the switch (e.g., Figure 3A, 3B).

Munguia discloses keeping track of latency times of selected processors, but does expressly consider the option of not tracking individual latency times; however this feature is disclosed by Keller. Keller discloses a function of a plurality of requests, without keeping track of latency times of any selected processor (e.g., para. 43).

Munguia discloses the use of a latency statistic for determining when to decrease responsive to a second parameter (e.g., col. 7, lines 34-40), but does not expressly mention the particular specifics of counter comparing and resetting; however, this particular embodiment is disclosed by Keller. Keller discloses the second parameter and comparing the value in the counter to the second parameter (paragraph [0044], "unless a predetermined number of latencies indicate that a change is in order"); and when the value in the counter is equal to the value of the second parameter, decreasing the number of bus clocks between issuance of requests to the switch from microprocessors connected to the switched system by the amount equal to the number of bus clocks defined as the first parameter and resetting the value in the counter to zero (e.g., paragraph [0044], "change the retry latency if both of the previous latencies indicate" which counter is set to zero when the latency is increased).

It would have been obvious to combine Keller with Munguia because Keller teaches simpler implementations of determining when to decrease latencies using a statistic of previous latency data, which statistic was disclosed by Munguia but with the additional feature of tracking individual latency times. Therefore it would have been

obvious to one of ordinary skill in the art to combine Keller with Munguia to obtain the claimed invention.

Regarding claims 5 and 11, Munguia also discloses the first parameter is defined at system power-on (e.g., col. 8, lines 45-47).

Regarding claims 6 and 12, Munguia does not expressly mention the predetermined value of the second parameter at power on; however Keller discloses this detail. Keller discloses a predetermined number of latencies (e.g., paragraph [0044], "predetermined number").

Regarding claim 14, Munguia discloses issuing at least one request from the microprocessor to the system switch (e.g., col. 7, lines 63-64); responsive to a signal from the system switch indicating it lacks resources to process a command, increasing the number of bus clocks to wait between issuance of requests from microprocessors by the number of bus clocks defined as the first parameter; waiting the increased number of bus clocks between issuance of requests to the switch (e.g., Figure 3A, 3B).

Munguia discloses keeping track of latency times of selected processors, but does expressly consider the option of not tracking individual latency times; however this feature is disclosed by Keller. Keller discloses a function of a plurality of requests, without keeping track of latency times of any selected processor (e.g., para. 43).

Munguia discloses the use of a latency statistic for determining when to decrease responsive to a second parameter (e.g., col. 7, lines 34-40), but does not expressly mention the particular specifics of counter comparing and resetting; however, this particular embodiment is disclosed by Keller. Keller discloses the second parameter

and comparing the value in the counter to the second parameter (paragraph [0044], "unless a predetermined number of latencies indicate that a change is in order"); and when the value in the counter is equal to the value of the second parameter, decreasing the number of bus clocks between issuance of requests to the switch from microprocessors connected to the switched system by the amount equal to the number of bus clocks defined as the first parameter and resetting the value in the counter to zero (e.g., paragraph [0044], "change the retry latency if both of the previous latencies indicate" which counter is set to zero when the latency is increased).

It would have been obvious to combine Keller with Munguia because Keller teaches simpler implementations of determining when to decrease latencies using a statistic of previous latency data, which statistic was disclosed by Munguia but with the additional feature of tracking individual latency times. Therefore it would have been obvious to one of ordinary skill in the art to combine Keller with Munguia to obtain the claimed invention.

Response to Arguments

Applicant's arguments filed 7/19/2004 with respect to the rejection of claims 1-14 using Munguia have been considered but are moot in view of the new ground(s) of rejection.

In particular, Munguia discloses a record of selected processor addresses and transaction types (e.g., Fig. 4, "404: Address & Transaction Type Match?") which does not apply to the exclusionary recitation of the newly amended claims.

Applicant's arguments regarding Keller, which has been newly applied as a teaching reference in combination with Munguia supra, have been fully considered but they are not persuasive.

Applicant argues that Keller discloses "recording latencies or recent data transfer latencies to various switches, and then selecting a retry latency from two or more retry latencies, but there is no detail to suggest a tracking of the overall activity level of a switch itself and making a generalized determination of an appropriate delay latency for the switch" (p. 14). However, Keller does precisely track overall activity; for example, "latency buffer 38 may store the first data transfer latencies of the most recent N read transactions.... The number of latencies stored in latency buffer 38 may be at least one, and is generally a positive integer. The number of latencies may be selected according to design choice. Larger numbers of latencies may provide a more accurate portrayal of the latencies currently being experienced by the system, but may also result in a slower reaction by retry circuit 30 to changing latency conditions" (para. 43). In this passage it is quite clear that stored latencies are not for "any selected processor or proxy processor" and therefore does not render Keller deficient with regard to the exclusionary language of the recitation.

Keller stores latencies, but indeed for any system that retries a request a latency must be stored because an elapsed time, or rate, between the initial request and its

retry must exist. For example, in the Applicant's specification, "COMPACE 50, is defined in the bus parameters, and stored in a register on the processor. COMPACE 50 is the basic unit used to vary the command issue rate to the bus 114." (p. 6, lines 26-28). COMPACE by the Applicant's definition corresponds to a latency between request and retry. For consistency between this feature and the claim language, the exclusion of latency storage as newly recited must refer to actual latency between a request and the availability of the response. Indeed, the Applicant's invention does not store this value, but neither does Keller. Keller sets minimum, nominal, and maximum latencies, which correspond to possible values for COMPACE. Keller discloses, "[t]he nominal retry latency may be initially selected by retry circuit 30, and may be just greater than the normally expected first data transfer latency for a transaction targeting a device on bus 24" (para. 39), which corresponds to Applicant's disclosure that "COMPACE 50 is programmed at power-on to specify the number of bus clocks between issue of commands to the bus 114 (p. 6, line 28 – p. 7, line 1). Keller likewise contemplates storage of latency in number of clock cycles (para. 45). What is, in effect, "stored" by Keller is a function of the number of retries, by which means Keller determines whether to increase the latency of the retry circuit; this corresponds to the Applicant's COMPACE register, which is likewise modified as a function of the number of retries. Therefore, Keller, in this interpretation is deemed anticipatory of the claimed invention as interpreted in a manner consistent with the Applicant's specification.

Regarding claim 4, Applicant further argues that the recitation "excludes use of a proxy processor as an alternative to tracking the latency times of individual processors.

In tracking overall use of the switch instead of a proxy processor, apparatus complexity is simplified" (p. 14); however, as noted supra, the exclusionary language refers to "not keep[ing] track of latency times of any selected processor or proxy processor" which interpreted in a manner consistent with the specification fails to exclude Keller.

Therefore the new rejection above using Munguia in view of Keller is deemed proper.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

Khanh Dang
Primary Examiner